EE105
Microelectronic Devices and Circuits:
P-N Junctions and Semiconductor Fabrication

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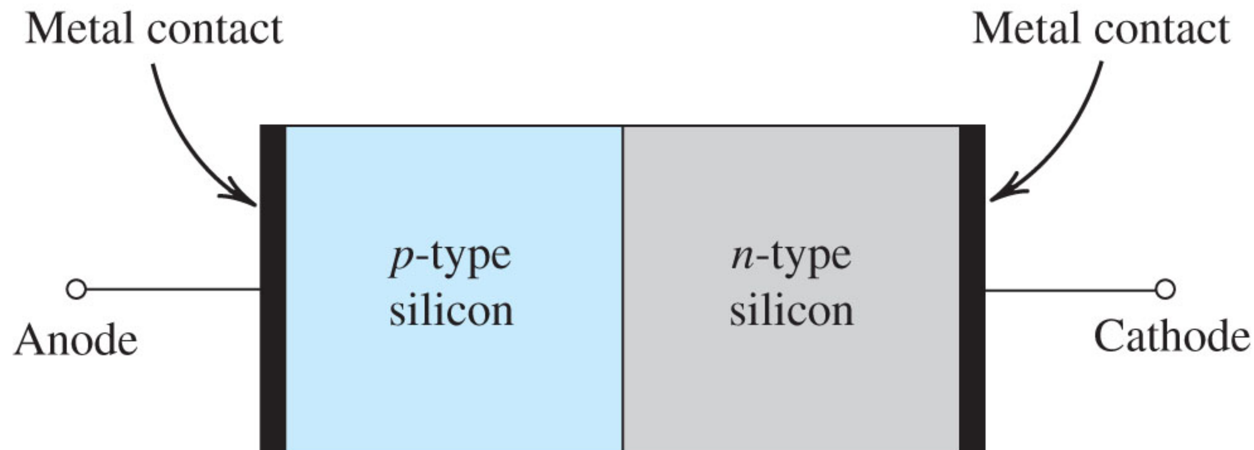
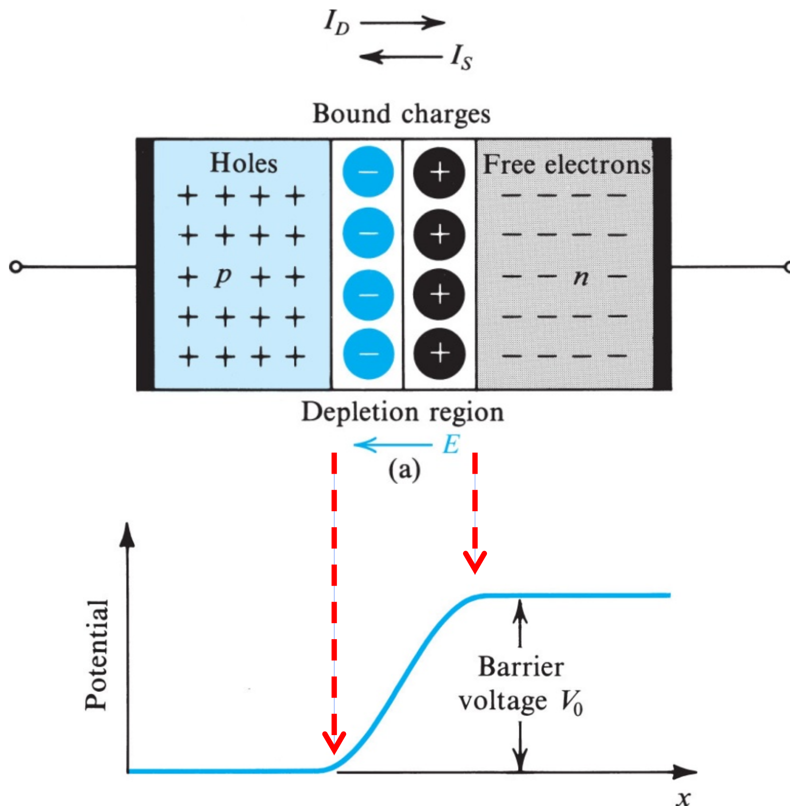
p-n Junction

- p-type semiconductor in contact with n-type
- Basic building blocks of semiconductor devices
  - Diodes,
  - Bipolar junction transistors (BJT),
  - Metal-oxide-semiconductor field effect transistors (MOSFET)

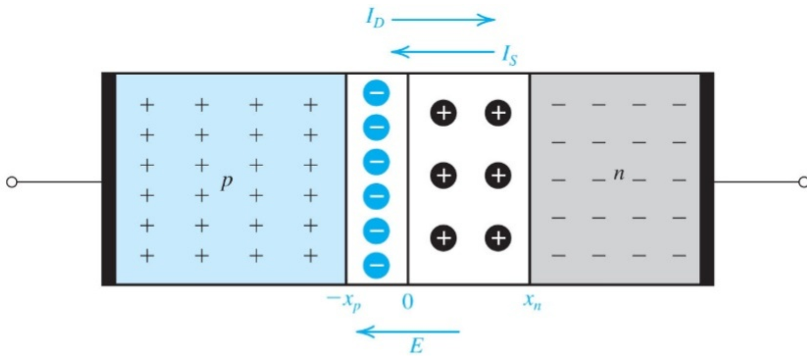


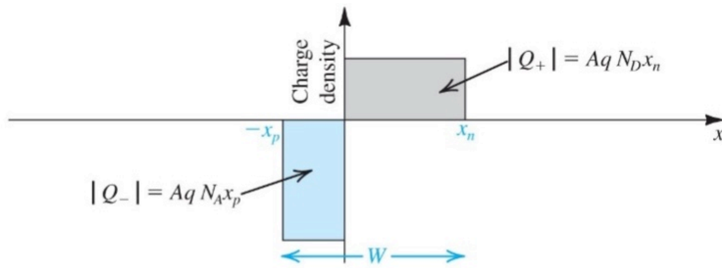
p-n Junction

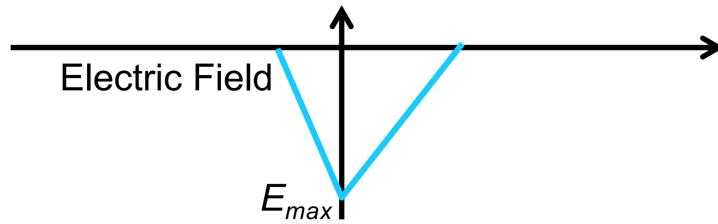


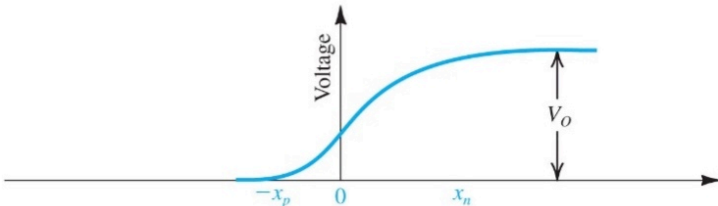
- When p- and n-type semiconductors are "joined"
  - Holes near junction diffuse to n-side
  - Electrons near junction diffuse to p-side
- "Depletion region" formed near junction
  - No electrons, no holes
- A "built-in" potential is formed to oppose further movement of electrons and holes

Simplified Analysis of p-n Junction









Gauss Law:

$$\oint \vec{E} \cdot \overrightarrow{dA} = \frac{Q}{\epsilon_s}$$

Electrical potential:

$$V = -\int_{-\infty}^{x} E(x')dx'$$

Built-in potential:

$$V_0 = V_T \cdot ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Depletion width:

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

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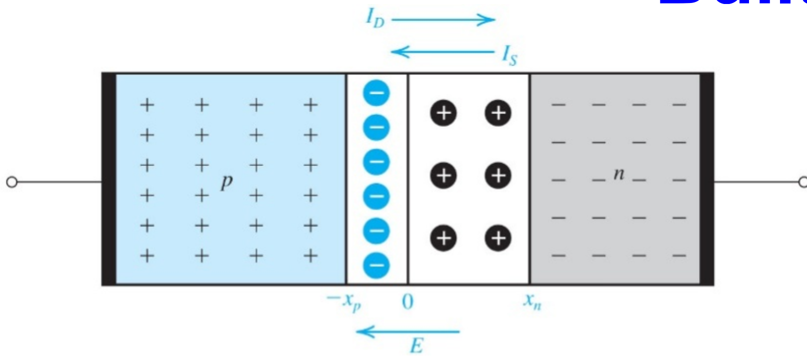
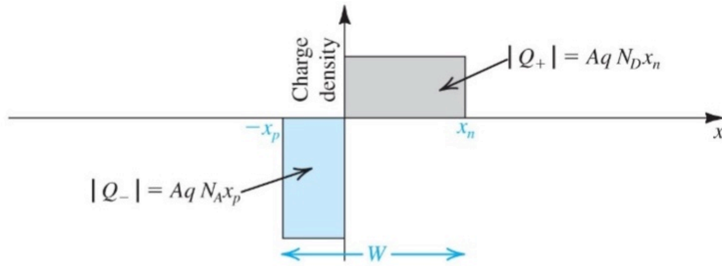
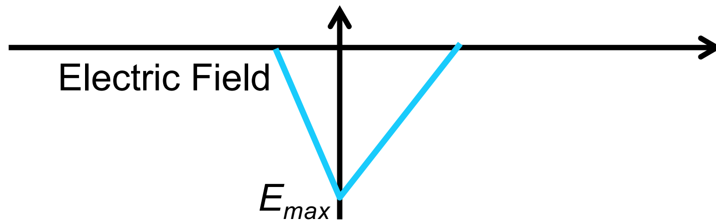
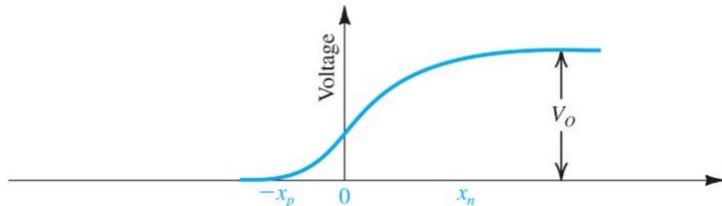
Built-in Potential









Built-in potential:

$$V_0 = V_T \cdot ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$V_T = \frac{k_B T}{q}$: thermal voltage = 26 mV at room temperature

N_A : p-doping (Acceptor)

N_D : n-doping (Donor)

n_i : intrinsic carrier concentration

$n_i = 1.5\times10^{10}\ cm^{-3}$ for Si

Alternative form:

$$V_0 = 60mV \cdot log\left(\frac{N_A N_D}{n_i^2}\right)$$

Example:

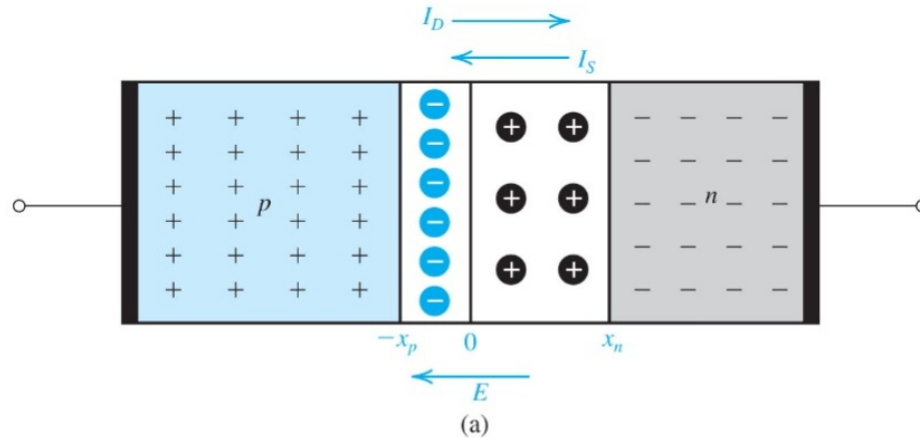
$N_A = 1.5\times10^{17}$, $n_D = 1.5\times10^{18}$ cm-3

$V_0 = 60mV \cdot log(10^{15}) = 900mV$

Carrier Concentration in p-n Junction

At equilibrium:

$$n \times p = n_i^2$$



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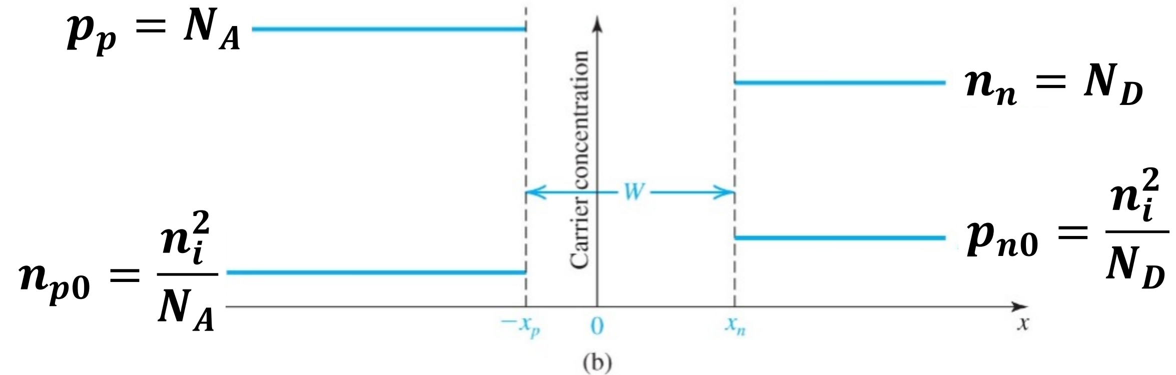
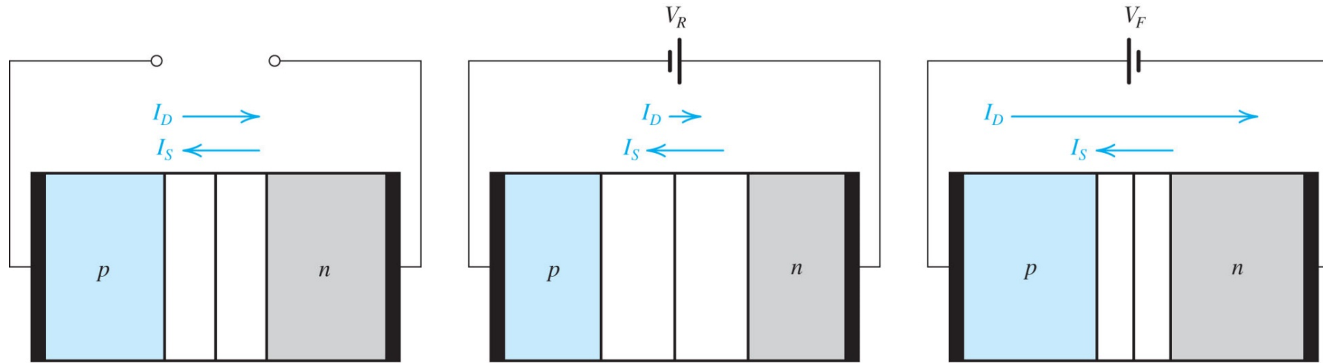


(b)

Depletion Width Under Bias



V_0 | $(V_0 + V_R)$ | $(V_0 - V_F)$

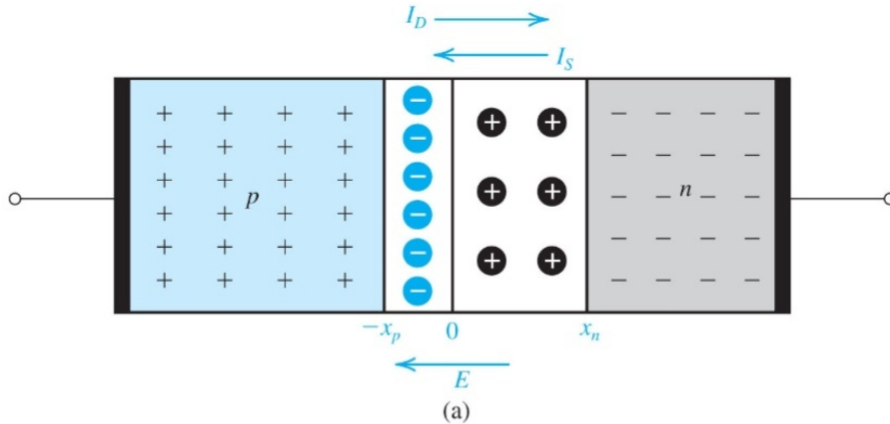
Open circuit
(V = 0)
Equilibrium

Reverse Bias
(V < 0)
- **Larger barrier**
- **Wider depletion**

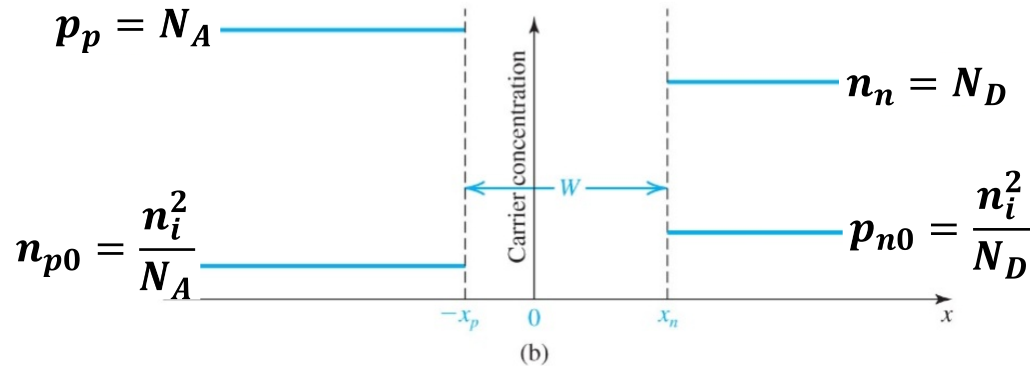
Forward Bias
(V > 0)
- **Smaller barrier**
- **Narrower depletion**

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 - V)}$$

Extra Holes in N Side Under Forward Bias



(a)

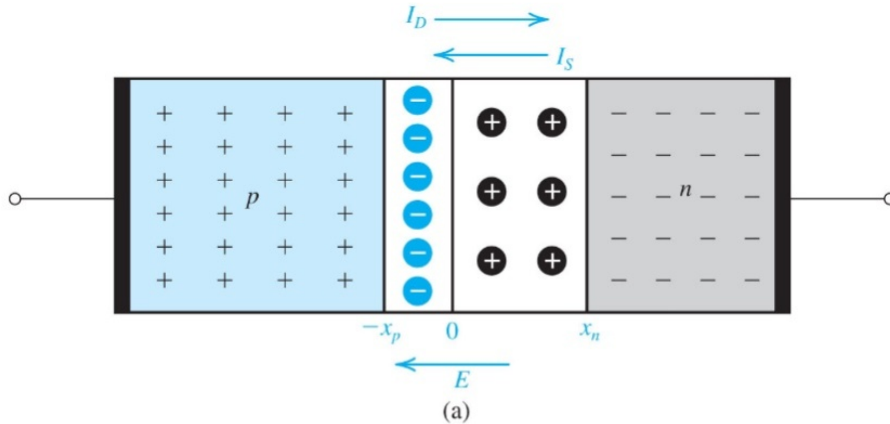


(b)

Excess holes in n-doped side:

$$p_{n,edge} = p_{n0} \cdot \left(e^{V/V_T} - 1\right)$$

Holes Recombine with Electrons on N Side



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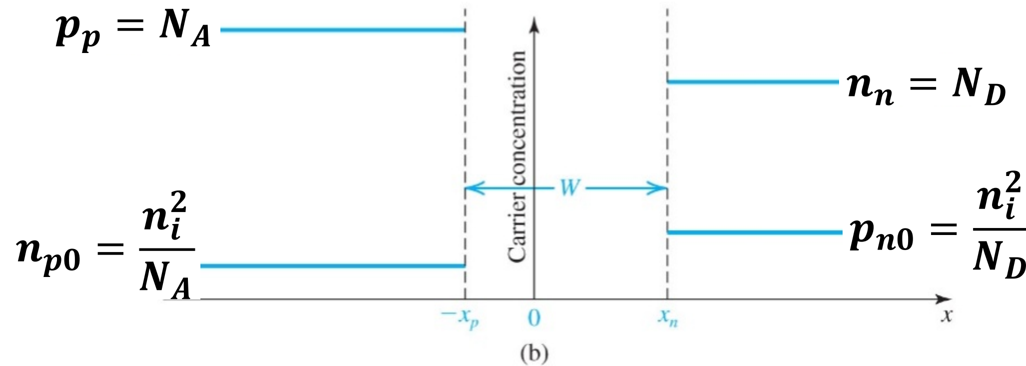


(b)

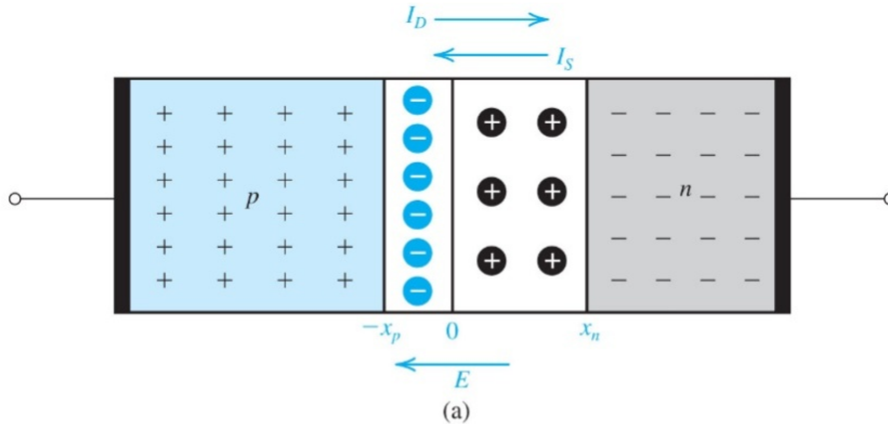
Excess holes in n-doped side:

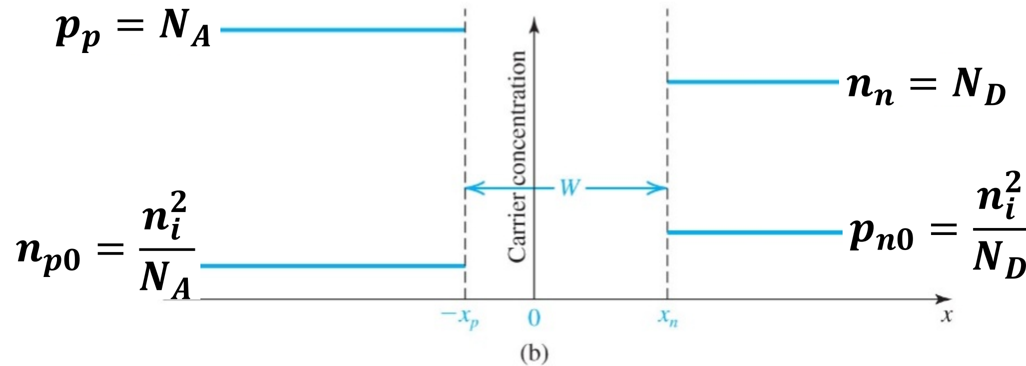
$$p_{n,edge} = p_{n0} \cdot \left(e^{V/V_T} - 1\right)$$

Excess holes recombines within diffusion length, L_p:

$$\frac{dp_n(x)}{dx} = \frac{p_{n,edge}}{L_p}$$

Diffusion Currents Under Forward Bias





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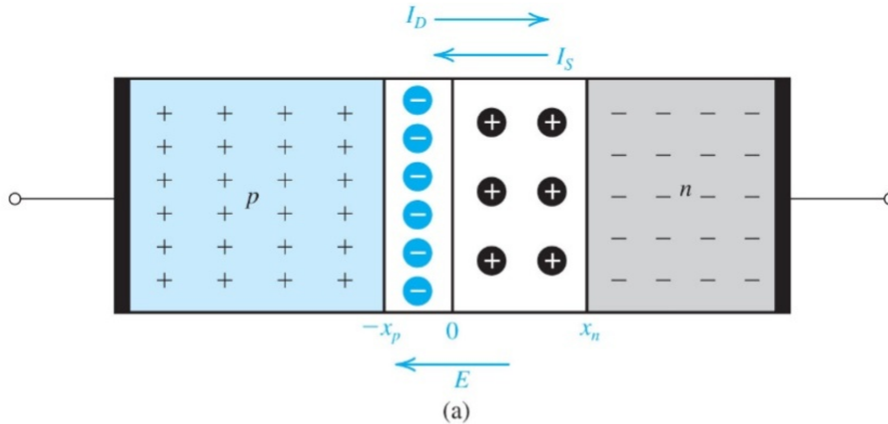
Diffusion current:

$$J_p = -qD_p \frac{dp_n(x)}{dx}$$
$$= \frac{qD_p}{L_p} p_{n0} \cdot \left(e^{V/V_T} - 1\right)$$

Total Currents Under Forward Bias



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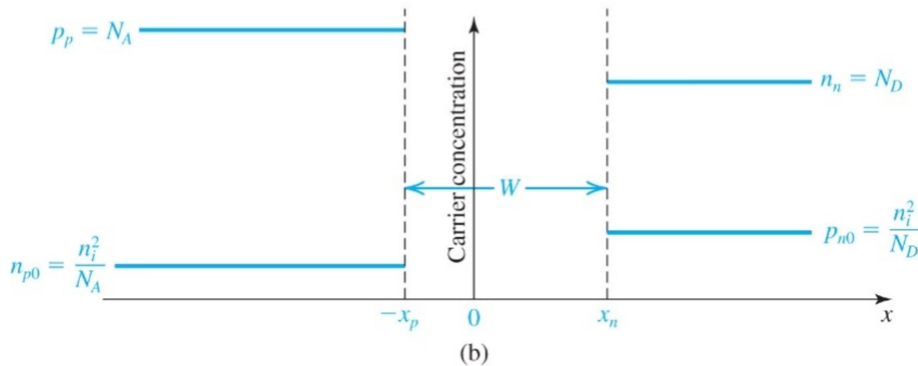


(b)

Hole Diffusion current on N-side

$$J_p = \frac{qD_p}{L_p} p_{n0} \cdot \left(e^{V/V_T} - 1\right)$$

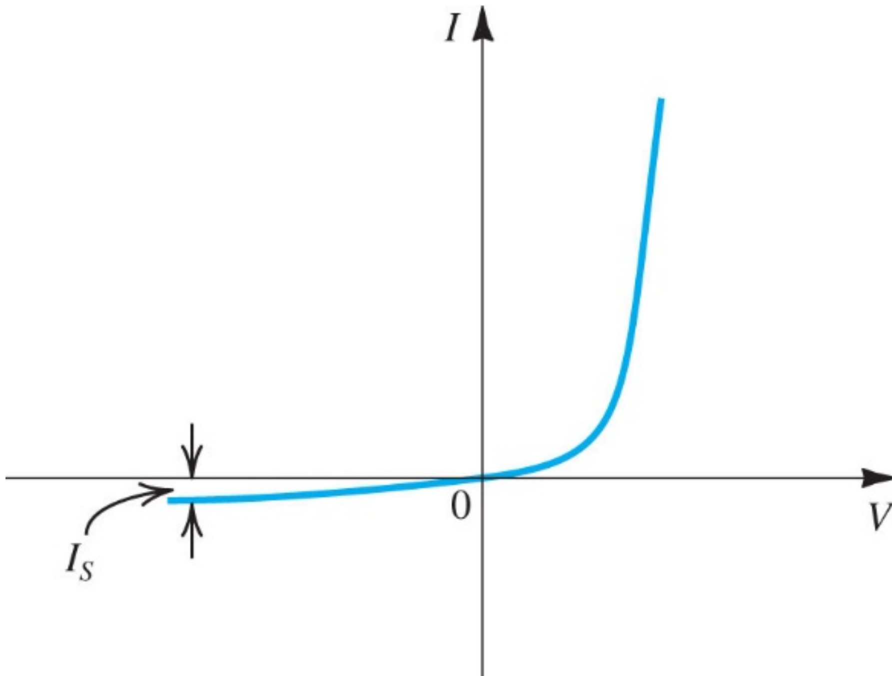
Similarly,
Electron Diffusion current on P-side

$$J_n = \frac{qD_n}{L_n} n_{p0} \cdot \left(e^{V/V_T} - 1\right)$$

Total current

$$I = Area \cdot (J_p + J_n) \propto \left(e^{V/V_T} - 1\right)$$

I-V Curve



$$I = I_S\left(e^{V/V_T} - 1\right)$$

where

$$I_S = Aqn_i^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)$$

Capacitance in p-n Junction: Depletion Capacitance

Parallel plate capacitance:

$$C_j = \frac{\epsilon_s A}{W}$$

Plate separation, *W*, is voltage dependent:

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + |V_R|)}$$

Variable capacitance:

$$C_j(V) = \frac{C_{j0}}{\sqrt{1 + \frac{|V_R|}{V_0}}}$$

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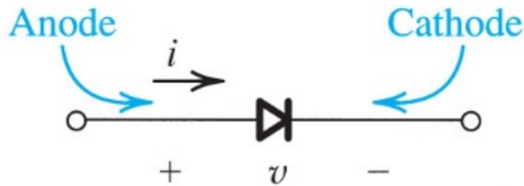
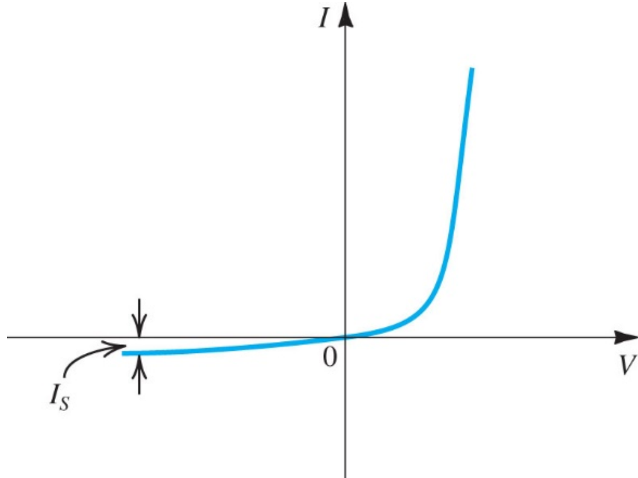
Summary of p-n Junction



Built-in potential : $V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$



I-V curve : $I = I_S\left(e^{V/V_T} - 1\right)$

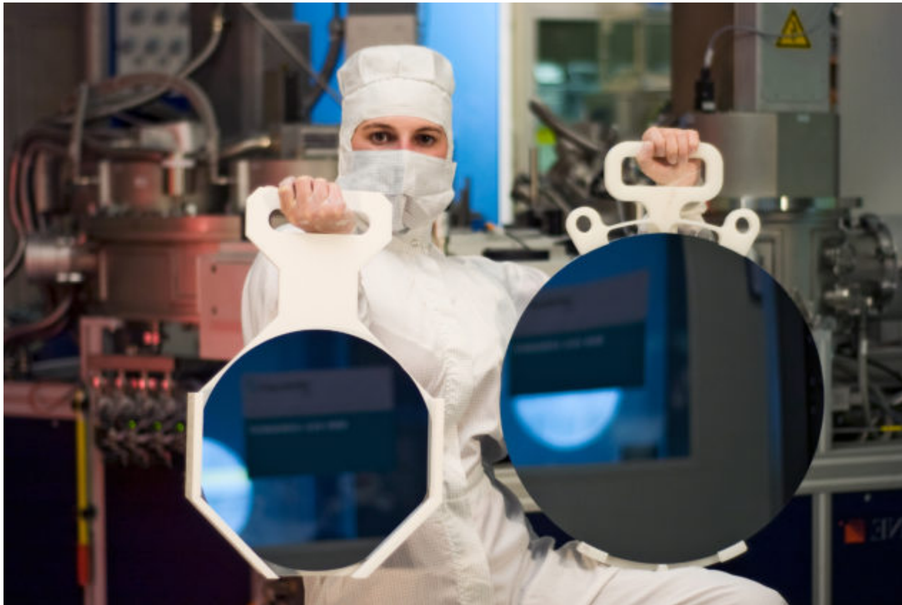
Capacitance : $C_j = \frac{C_{j0}}{\sqrt{1 + \frac{|V_R|}{V_0}}}$

Depletion Width: $W = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\left(V_0 - V\right)}$

Basic Semiconductor Fabrication

Economy of Scale

300mm and 450mm Si Wafers

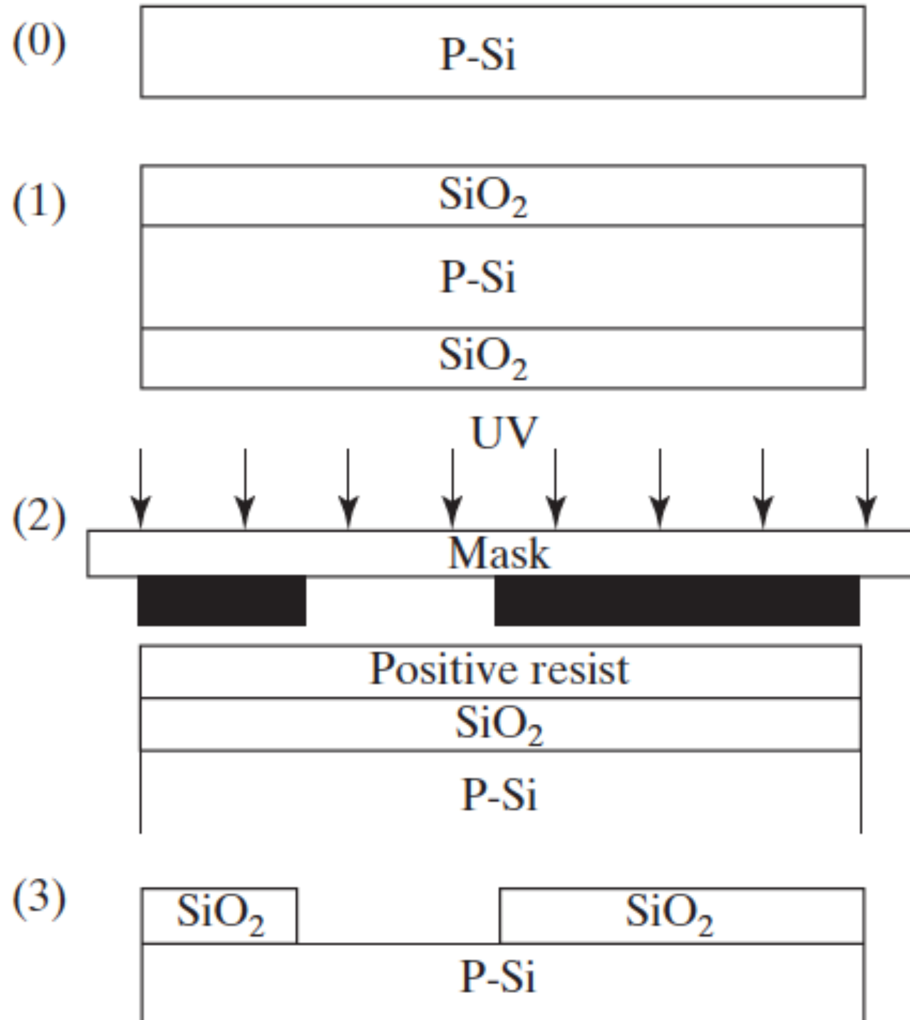


http://wccftech.com/foundries-tsmc-companies-shift-300mm-wafers/

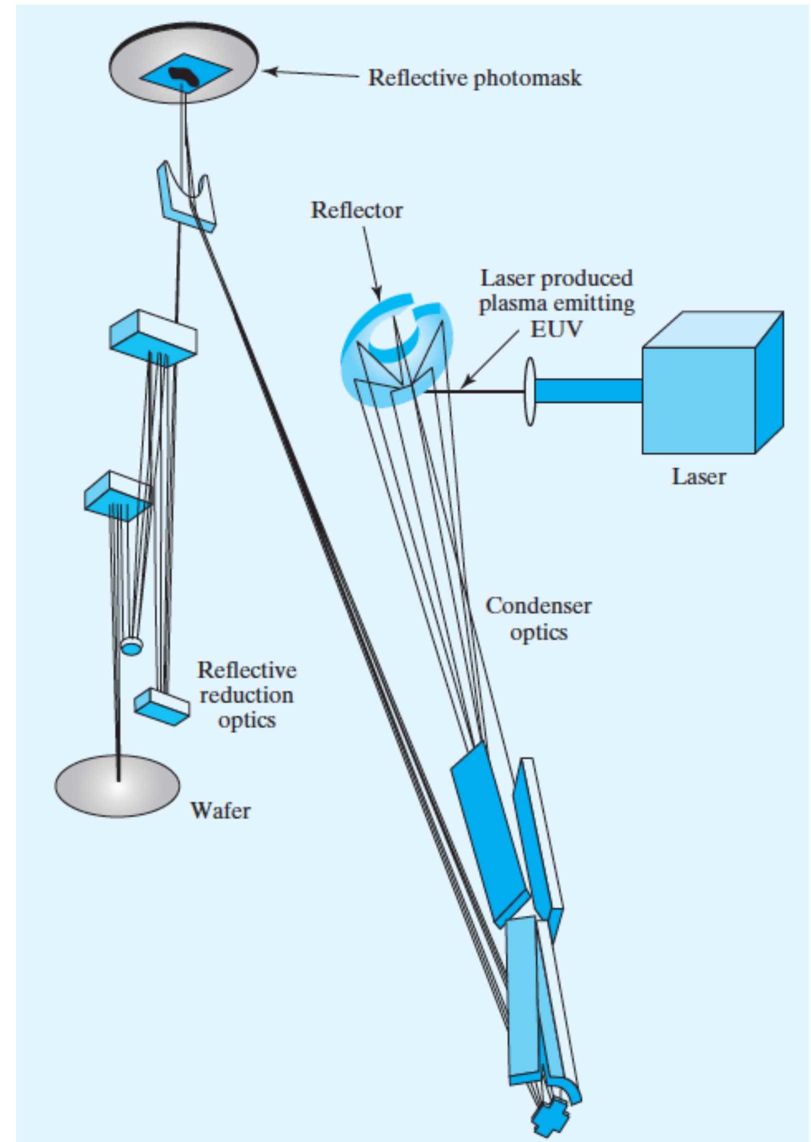
- **Current: 300mm wafers**
- **Next gen: 450mm wafers**
- **200mm wafers are still workhorse, particularly for IoT**
- **Economy of scale**
  - **Full CMOS has 60+ photomasks, and yet chip cost almost nothing**
  - **$1K for 200mm**
    - **\$ /mm²**
  - **$10K for 300mm**
    - **\$ /mm²**

Basic Semiconductor Fabrication Process

Learn more in EE 143



State of the Art Lithography Machine
(EUV: Extreme Ultra Violet)



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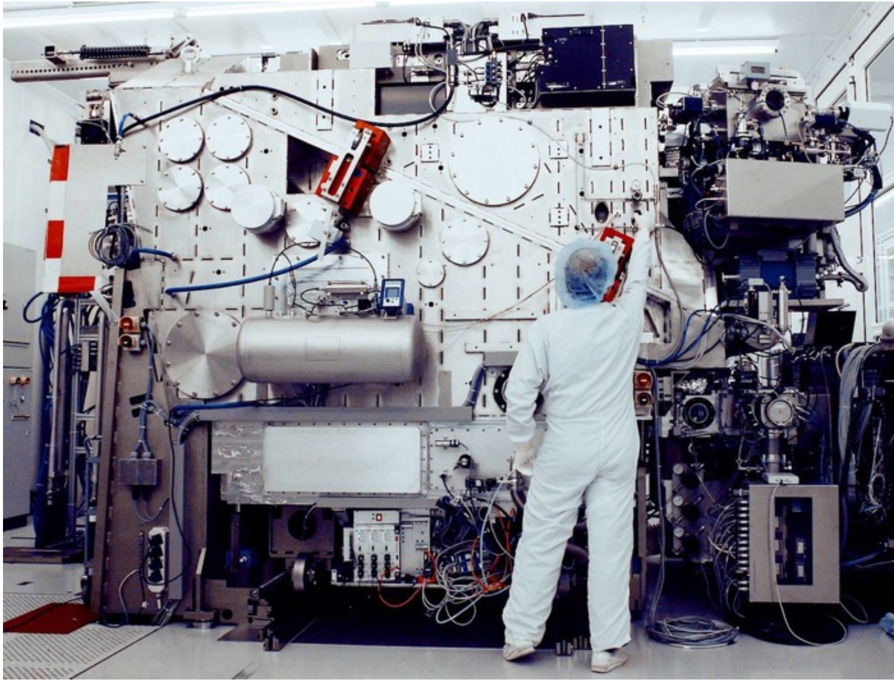
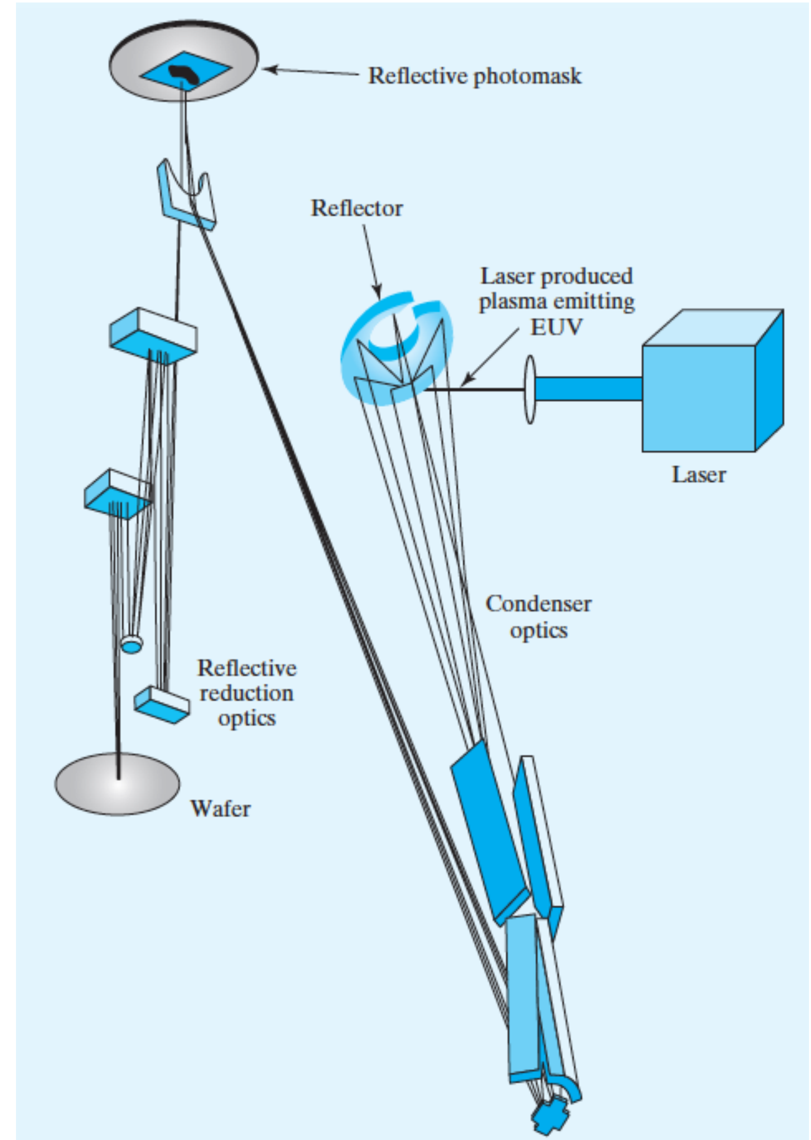
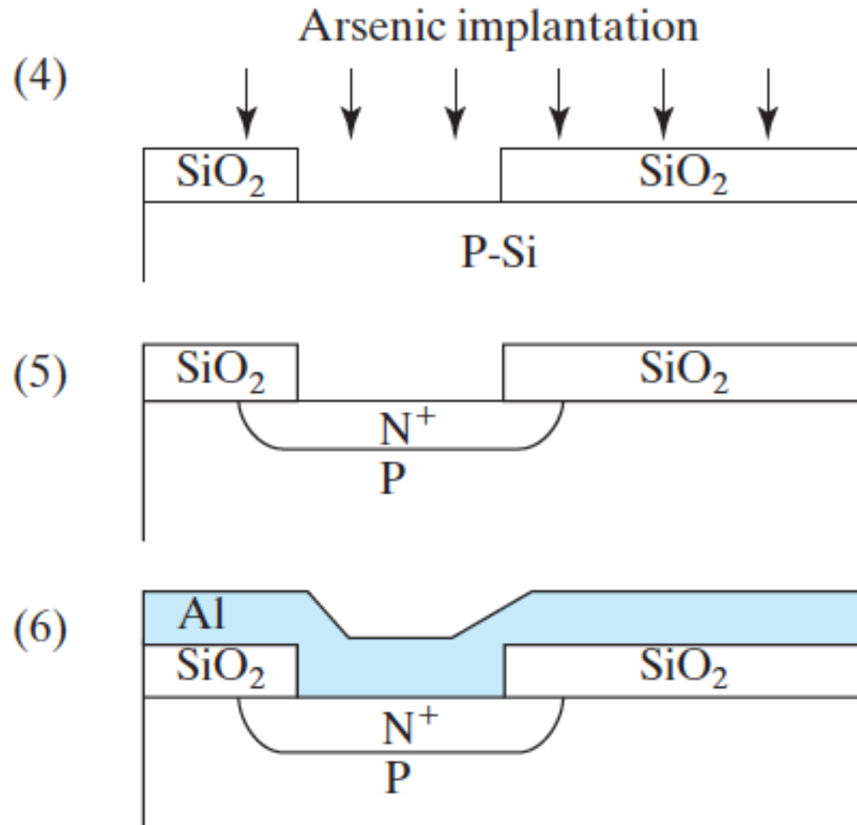
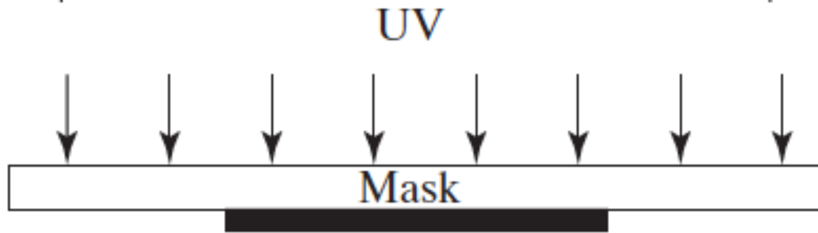


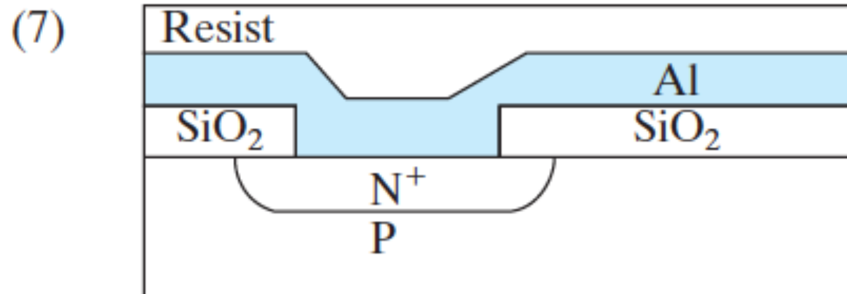


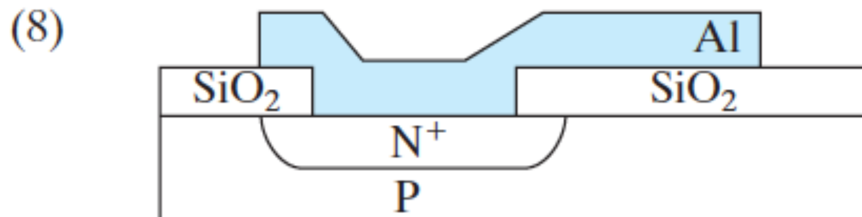
Microfabrication (cont'd)



Microfabrication (cont'd)







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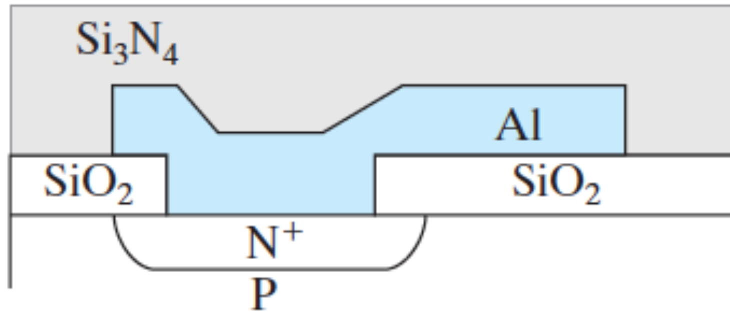
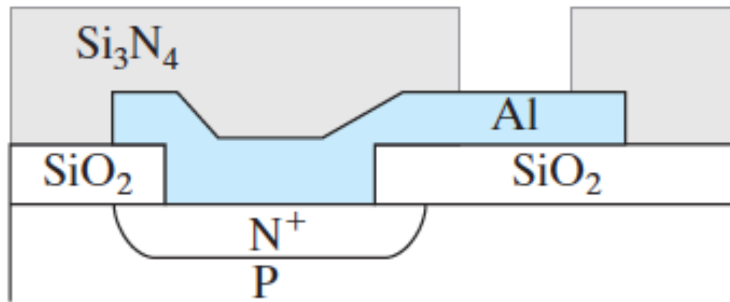
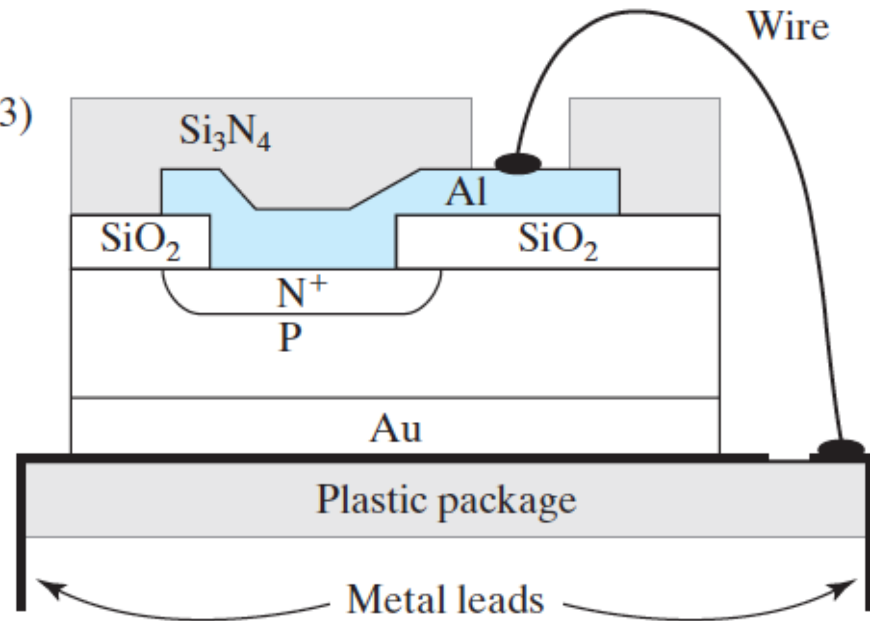
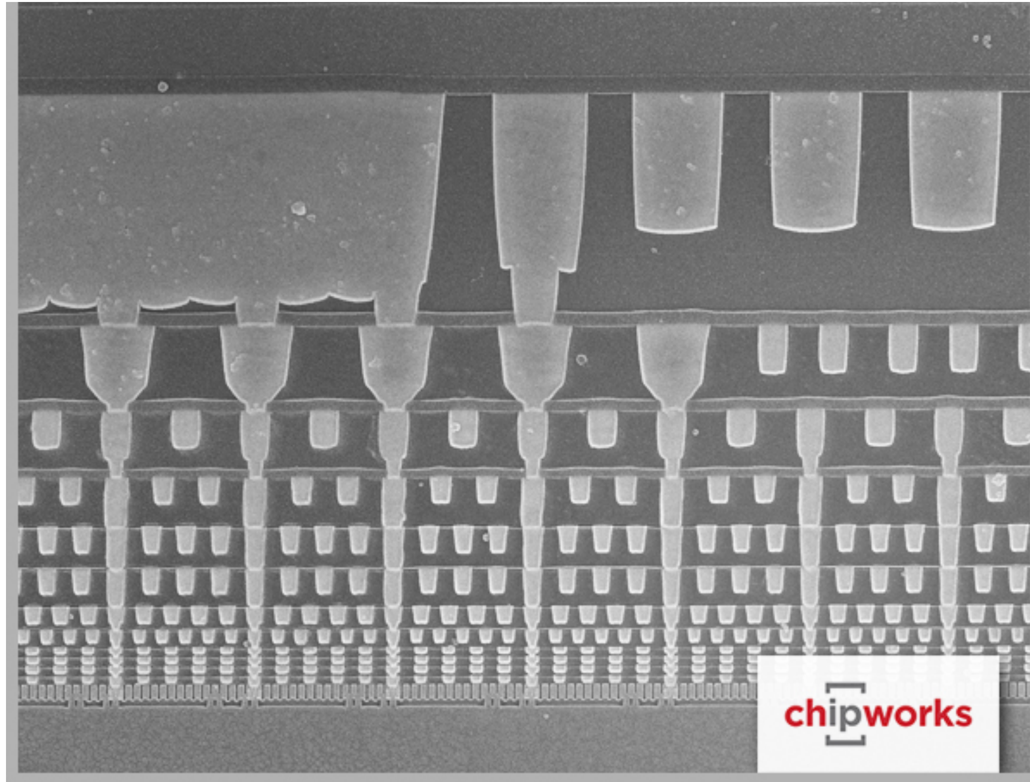






Modern CMOS IC Cross Section



Intel 14nm Broadwell chip, side-on, showing all 13 layers

Appendix

- Rigorous derivation of pn junction potential
- Rigorous derivation of junction capacitance

Rigorous Derivation of pn Junction Potential

$$E(x)=\begin{cases}\dfrac{-qN_A(x+x_p)}{\varepsilon_S}, & -x_p<x<0\\ \dfrac{qN_D(x-x_n)}{\varepsilon_S}, & 0<x<x_n\end{cases}$$

$$V(x)=-\int_{-x_p}^{x}E(x')dx'$$

(1) for $-x_p<x<0$: $V(x)=-\int_{-x_p}^{x}E(x')dx'=\int_{-x_p}^{x}\frac{qN_A(x'+x_p)}{\varepsilon_S}dx'=\frac{qN_A}{2\varepsilon_S}\left(x'+x_p\right)^2\Big|_{x'=-x_p}^{x'=x}=\frac{qN_A}{2\varepsilon_S}\left(x+x_p\right)^2$

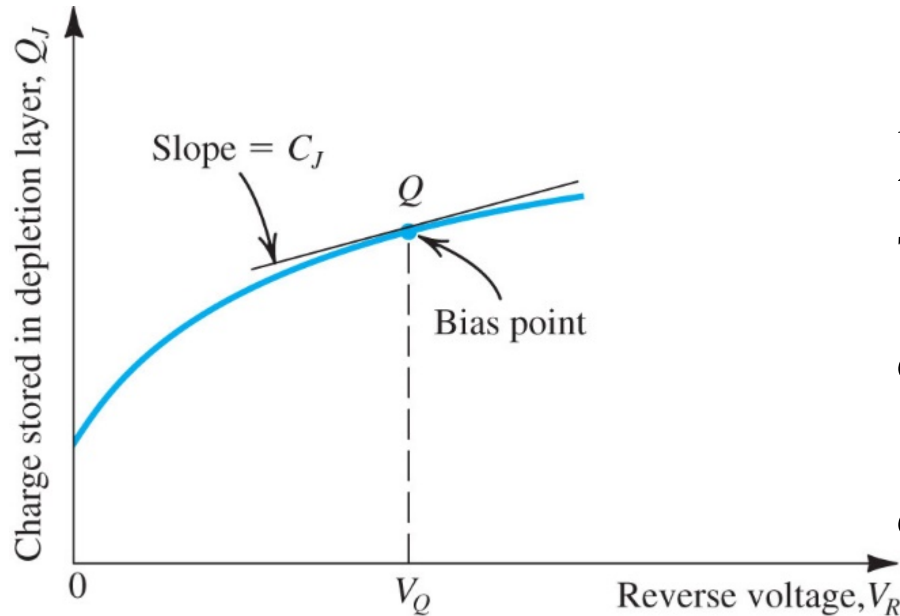
(2) for $0<x<x_n$: Because $E(x)$ has different expression for $x<0$ and $x>0$, the integration should be performed in two separate ranges, first from $-x_p$ to 0, and then from 0 to x. We can use $V(x=0)$ from the above equation for the first intgration. Therefore,

$$V(x)=\frac{qN_A}{2\varepsilon_S}x_p^2-\int_0^x\frac{qN_D(x'-x_n)}{\varepsilon_S}dx'=\frac{qN_A}{2\varepsilon_S}x_p^2-\frac{qN_D(x'-x_n)^2}{2\varepsilon_S}\Big|_0^x$$

$$=\frac{qN_A}{2\varepsilon_S}x_p^2-\left(\frac{qN_D(x-x_n)^2}{2\varepsilon_S}-\frac{qN_Dx_n^2}{2\varepsilon_S}\right)=\frac{qN_A}{2\varepsilon_S}x_p^2+\frac{qN_Dx_n^2}{2\varepsilon_S}-\frac{qN_D(x-x_n)^2}{2\varepsilon_S}$$

Built-in potential: $V_0=V(x_n)=\frac{q}{2\varepsilon_S}\left(N_Ax_p^2+N_Dx_n^2\right)$

Rigorous Derivation of Junction Capacitance



In comparision, for a "linear" (normal) capacitor:

$C = \dfrac{Q}{V}$ is a constant

Total charge Ain depletion width at $V = -V_R$

$$Q_J = AqN_D x_n = AqN_D \frac{N_A}{N_A + N_D} W$$

$$W = \sqrt{\frac{2e_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$$

As bias voltage change, the amount of charge in the junction change. This is a "nonlinear" capacitor. The capacitance value is

$$C_j = \frac{dQ_J}{dV_R} = Aq\frac{N_D N_A}{N_A + N_D}\sqrt{\frac{2e_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}\frac{d}{dV}\sqrt{(V_0 + V_R)}$$

$$C_j = A\sqrt{\frac{\varepsilon_S q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)}\frac{1}{\sqrt{(V_0 + V_R)}}$$

Note: $C_j = \dfrac{\varepsilon_S A}{W}$

At zero bias, $V_R = 0$

$$C_{j0} = A\sqrt{\frac{\varepsilon_S q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)}\frac{1}{\sqrt{V_0}}$$

Therefore at $V = -V_R$,

$$C_j = \frac{C_{j0}}{\sqrt{1 + \dfrac{V_R}{V_0}}}$$

This is a variable capacitor, controllable by voltage !

Cal

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